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TITLE: LDD mosfet mfr. by forming overlap of fixed thickness under electrode -
by forming diffusion area with low impurity concn. by diffusing impurity by
pyrogenic heat treatment NoAbstract Dwg 1/1

PATENT-ASSIGNEE: KAWASAKI STEEL CORP[KAWI]

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METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE
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Specification /1[1]

1. Title of the Invention: METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE

2. Claim

A method for manufacturing a semiconductor device which includes

A process whereby a gate electrode which consists of polysilicon is formed on the surface of a semiconductor substrate of a given electroconductivity type via a gate insulating film,

A process whereby a film of a high-melting-point metal such as tungsten, titanium, etc. is formed above said gate electrode and whereby a metal silicide film is subsequently formed above the surface of said gate electrode by means of a thermal treatment,

A process wherein an impurity of the other electroconductivity type is implanted into said semiconductor substrate while said metal silicide film and gate electrode avail themselves as masks,

A process whereby said semiconductor substrate is subjected to a high-temperature thermal treatment in an oxygen atmosphere or the atmosphere of oxygen diluted with an inert gas for forming a diffusion layer of a low impurity concentration by means of the diffusion of the implanted impurity based on its accelerated oxidative diffusion underneath said gate electrode in such a way

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[1]Numbers in the margin indicate pagination in the foreign text.

that an overlap margin of at least 0.05 μm will be achieved,

A process whereby a side wall which serves a mask function against the ion implantation is formed on the profile plane of said gate electrode, and

A process whereby an impurity of the second electroconductivity type is implanted and diffused at a high concentration for forming a source and a drain while said metal silicide film, gate electrode, and side wall are being used as masks.

3. Detailed explanation of the invention

(Industrial application fields)

The present invention concerns a method for manufacturing a semiconductor device, and more specifically, it concerns a method for manufacturing a MOSFET of an LDD structure the drain of which is constituted by a low-impurity-concentration region and a high-impurity-concentration region.

(Prior art)

As far as MOSFETs of the prior art characterized by microscopic structures are concerned, an LDD (lightly doped drain) structure wherein a diffusion layer of a low impurity concentration (n^- layer [or?] p^- layer) is sandwiched between a source/drain diffusion layer and a channel region is being used generally and extensively for the purpose of inhibiting hot carrier effects, etc. As far as such a MOSFET of the LDD structure is concerned, it is impossible to sufficiently diffuse the impurity in its low-impurity-concentration diffusion layer /2

due very to said low concentration, and since its diffusion along the lateral direction is accordingly minimal, it cannot be sufficiently doped into the area underneath the gate electrode. There is therefore no sufficient overlap between the $^-$ layer and the gate electrode. In recent years, the channel resistance has come to be lowered in accordance with short-channel trends, and accordingly, the parasitic resistance has become no longer negligible. In a case where the overlap margin between the gate electrode and the $^-$ layer is sufficient, the hot carrier resistance diminishes, accompanied by a transistor parasitic resistance gain, which is problematic in that the current drive capacity diminishes. As a result of the post-oxidation treatment of the polysilicon that constitutes the gate electrode, furthermore, the side wall of the gate electrode becomes oxidized, which makes it more difficult to secure the requisite overlap between the gate electrode and $^-$ layer. A gate/n^- overlap LDD structure wherein a gate electrode and a low-impurity-concentration diffusion layer (e.g., $^-$ layer) are orchestrated to overlap has come to be proposed for eliminating these shortcomings and for improving the hot carrier resistance and the current drive capacity while the generation of a parasitic resistance is being inhibited, an example of which is mentioned in IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 35, No. 12, pp. 2088 ~ 2093, which was published in December 1988.

(Problems to be solved by the invention)

As far as the gate-drain overlapped device (GOLD) mentioned

in the aforementioned IEEE TRANSACTIONS ON ELECTRON DEVICES is concerned, an oxide layer is formed above a polysilicon film, followed by the under-etching of the polysilicon film for forming a trapezoidal gate electrode with an extended tapered span, and phosphorus is subsequently implanted ionically into it for forming an $^-$ layer which stretches itself all the way to the bottom of the tapered portion of the gate electrode and for securing an overlap, followed by the formation of side walls on the profile planes of the gate electrode and oxide film, and an n^+ layer is then formed by ionically implanting arsenic at a high concentration. Such a method, however, requires complicated processes, which is problematic in that cost increases become unavoidable and that it becomes difficult to control the dimensions and shape.

The ion implantation of a low-impurity-concentration layer has come to be executed more deeply at a higher energy in recent years in the context of further improving the hot carrier resistance, and accordingly, the problem of the overlap has become increasingly more grave. During a thermal treatment for diffusing the implanted ion, furthermore, the polysilicon that constitutes the gate electrode becomes concomitantly oxidized, but since the oxidation rate of the polysilicon is high, the gate electrode (electroconductive layer portion[)] becomes thin, as a result of which the optical band gap between the $^-$ layer and gate electrode further diminishes.

The objective of the present invention, which has been

conceived for eliminating the aforementioned shortcomings of the prior art, is to provide a method for manufacturing a semiconductor device which is capable of securing a sufficient overlap margin between a low-impurity-concentration diffusion layer and a gate electrode with regard to the MOSFET of the LDD structure and of achieving a high yield based on simple processes.

(Mechanism for solving the problems and functions)

The method of the present invention for manufacturing a semiconductor device includes

A process whereby a gate electrode which consists of polysilicon is formed on the surface of a semiconductor substrate of a given electroconductivity type via a gate insulating film,

A process whereby a film of a high-melting-point metal such as tungsten, titanium, etc. is formed above said gate electrode and whereby a metal silicide film is subsequently formed above the surface of said gate electrode by means of a thermal treatment,

A process wherein an impurity of the other electroconductivity type is implanted into said semiconductor substrate while said metal silicide film and gate electrode avail themselves as masks,

A process whereby said semiconductor substrate is subjected to a high-temperature thermal treatment in an oxygen atmosphere or the atmosphere of oxygen diluted with an inert gas for forming a diffusion layer of a low impurity concentration by means of the

diffusion of the implanted impurity based on its accelerated oxidative diffusion underneath said gate electrode in such a way that an overlap margin of at least 0.05 μm will be achieved,

A process whereby a side wall which serves a mask function against the ion implantation is formed on the profile plane of said gate electrode, and

A process whereby an impurity of the second electroconductivity type is implanted and diffused at a high concentration for forming a source and a drain while said metal silicide film, gate electrode, and side wall are being used as masks.

As far as such a method of the present invention is concerned, an ion is implanted for forming a low-impurity-concentration diffusion layer, and subsequently, a high- /3
temperature thermal treatment is performed in an oxygen atmosphere or the atmosphere of oxygen diluted with an inert gas for inducing accelerated oxidative diffusion, based on which the impurity can be diffused at a diffusion coefficient 4 to 5 times higher than that of an ordinary diffusion process, and since it can be diffused deeply underneath the gate electrode, a sufficient overlap margin vis-a-vis the gate electrode can be secured. Since the surface of the gate electrode is covered with a metal silicide film which serves as an oxidation-resistant film prior to the ion implantation and accelerated oxidative diffusion, furthermore, the oxidation and bulging of the gate electrode surface can be prevented during the accelerated

oxidative diffusion treatment, based on which the thinning of the electrode portion can be avoided while the loss of the overlap margin between the gate electrode and low-impurity-concentration diffusion layer is being avoided.

(Application examples)

Figures 1 show the constitution of a semiconductor device in the respective processes of an application example of the method of the present invention for manufacturing a semiconductor device in proper order. First, as Figure 1A indicates, the silicon oxide film (2), which constitutes a gate insulating film, is uniformly formed on the surface of the P-type silicon semiconductor substrate (1) at a thickness of 200 Å, and after a polysilicon film with a thickness of 4,000 Å has subsequently been deposited on it based on the CVD method, it is patterned and processed by means of photoetching, as a result of which the gate electrode (3) is formed. Next, as Figure 1B indicates, a film of a high-melting-point metal such as tungsten, titanium, etc. (titanium film (4) in the present example) is deposited on the surface of said gate electrode. Next, as Figure 1C indicates, a thermal treatment is performed within a temperature range of 800 ~ 850°C, as a result of which the titanium film (4) and the polysilicon of the gate electrode (3) become mutually reacted, and the titanium silicide layer (5) is formed. After the residual titanium film and silicon oxide film (2) above the diffusion layer have then been etched and removed, an oxidation treatment is performed, as a result of which the thin silicon

oxide film (7), the thickness of which is 100 Å, becomes formed on the surface of the silicon substrate (1). Next, as Figure 1D indicates, a phosphorus ion is implanted at an energy of 70 KeV while the gate electrode (3) and titanium silicide layer (5) are being employed as masks. The phosphorus ion concentration is concomitantly controlled at approximately 2 x 10^{13} atoms/cm^2. Next, the implanted phosphorus ion is diffused by means of accelerated oxidation based on annealing in an [undiluted] oxygen atmosphere or diluted oxygen atmosphere, as a result of which the $^-$ layers (8) and (9) are formed, as Figure 1E indicates. As far as the present example is concerned, said annealing is performed by thermally treating the semiconductor substrate (1) in a diluted oxygen atmosphere which has been obtained by internalizing 50% (in terms of the partial pressure ratio) of an inert gas (e.g., nitrogen, argon, etc.) into oxygen at a temperature of 900°C for approximately 1 hour. This accelerated oxidative diffusion can also be performed in an [undiluted] oxygen atmosphere, and in such a case, a thermal treatment is performed within a temperature range of 900 ~ 950°C for several dozen minutes. The phosphorus ion diffusion coefficient during such an accelerated oxidative diffusion is 4 to 5 times higher than that of an ordinary thermal diffusion process which is implemented in a non-oxidative atmosphere, and accordingly, it can be diffused over a sufficient depth underneath the gate electrode (3). In this case, satisfactory results are obtained so long as the $^-$ layers (8) and (9) overlap said gate electrode

over a distance of at least 0.05 μm. In such a case, the silicon oxide film (10), the thickness of which is several hundred Å, becomes formed above the diffusion layer, but since the titanium silicide layer (5) has been formed on the surface of the gate electrode (3), which is constituted by polysilicon, the gate electrode remains unoxidized, based on which the loss of the overlap margin between the gate electrode (6) and the $^-$ layers (8) and (9) can be avoided.

Next, as Figure 1F indicates, the side wall (11), which may, for example, be constituted by a silicon oxide film, is formed on the profile plane of the gate electrode (4) [sic: presumably "(3)"], which is being covered with the titanium silicide layer (5), and after an arsenic ion has been implanted by using said side wall as a mask, an ordinary thermal treatment is performed, as a result of which the source (12) and the drain (13), which are continuous with the $^-$ layers (8) and (9), become formed. Subsequent treatment procedures are similar to those for forming an ordinary MOSFET, and accordingly, no detailed explanations will be provided.

As has been mentioned above, as far as the present invention is concerned, the phosphorus ion is deeply diffused underneath the gate electrode (4) [sic] by means of accelerated oxidative diffusion in the context of forming a low-impurity-concentration diffusion layer. In such a case, the diffusion coefficient can be ascertained to be as follows according to the process simulator SUPREM (Stanford University Process Engineering Model):

$D = D_0 \times (1 + \text{Oed. fact}) \ldots (1)$.

In the above, D_0 signifies the diffusion coefficient in the absence of accelerated oxidative diffusion, whereas Oed. fact signifies a coefficient which is related to the accelerated oxidation. Said Oed. fact can be expressed by formula (2), which is shown below, and since its value is proportional to the oxidation rate raised to the 0.5th power, its value is extremely low in a non-oxidative atmosphere, whereas its value is high in an oxidative atmosphere: Oed. fact = [FII. O x exp(-FII. E/(kT)) x (OED. KO x exp(-OED. KE/(kT), x $dX_{max}/dt)^{\text{OED Rate}}$] ... (2). /4

In the above, the numerical parameters shown below are applicable in a case where one the plane orientation of which is (100) is employed as the silicon substrate (1) and where the arsenic ion is diffused by means of a thermal treatment in a dry oxygen atmosphere: FII. O = 5.50; FII. E = 0.57 eV; OED. KO = 2.86×10^{-16} min/μm; OED. KE = -5.64 eV; dX_{max}/dt = ~ 1 x 10; OED. RATE = 0.5; k = 8.36×10^{-5} eV/K; T = 1,173K.

Diffusion coefficient calculation results obtained by using these numerical parameters in a 900°C or 950°C dry oxidative atmosphere are shown in the following table.

Table

	Diffusion coefficient		
Temperature	In dry oxygen	In an inert gas	Multiple ratio
900°C	7×10^{-15}	1.4×10^{-15}	approx. 5 times
950°C	approx. 2×10^{-14}	approx. 5×10^{-15}	approx. 4 times

As the foregoing results indicate, the diffusion coefficient during the accelerated oxidative diffusion is 4 to 5 times higher than that of an ordinary diffusion process and that a sufficient overlap margin can be achieved since the phosphorus ion has become diffused all the way to the area underneath the gate electrode.

(Effects of the invention)

As has been mentioned above, as far as the method of the present invention for manufacturing a semiconductor device is concerned, an ion implantation operation for obtaining a low-impurity-concentration diffusion layer of the LDD structure is carried out by using a gate electrode as a mask, followed, if necessary, by restorative oxidation of the minimal magnitude, and after a high-temperature thermal treatment has been performed in an oxygen atmosphere or the atmosphere of oxygen diluted with an inert gas for enabling the diffusion of an ion deeply underneath the gate electrode by means of accelerated oxidative diffusion while restorative oxidation is being concomitantly induced, a low-impurity-concentration diffusion layer is formed. Since the polysilicon gate electrode is covered with a metal silicide film prior to said accelerated oxidative diffusion treatment, furthermore, the thinning of the gate electrode during the accelerated oxidative diffusion treatment can be avoided, and the loss of the gate-drain overlap margin can also be avoided. It is thus that a gate-drain overlap margin of at least 0.05 μm can be secured, and not only can the hot carrier resistance be improved,

but the current drive capacity can also be improved by mitigating the parasitic resistance. Since there is no need to configure a special layer or to implant ions diagonally for enlarging the overlap margin, furthermore, the complication of the manufacturing processes can be avoided, based on which the yield and reliability can be improved.

4. Brief explanation of the figures

Figures 1A through G are diagrams which show cross-sectional views of the respective processes of an application example of the method of the present invention for manufacturing a semiconductor device in proper order.

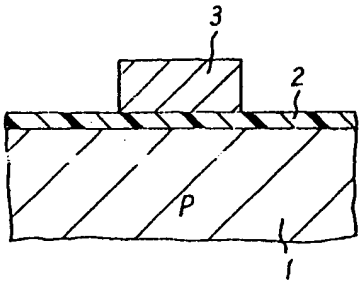
(1): Silicon semiconductor substrate; (2): Silicon oxide film; (3): Gate electrode; (4): Titanium film; (5): Titanium silicide layer; (6): Gate oxide film; (8) and (9): n^- layers; (10): Silicon oxide film; (11): Side wall; (12): Source; (12) [sic: Presumably "(13)"]: Drain.

Figure 1F

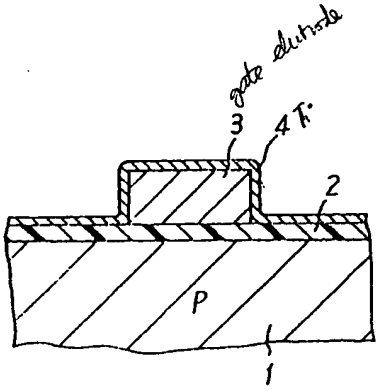
[(1): Phosphorus ion]

第 1 図

A

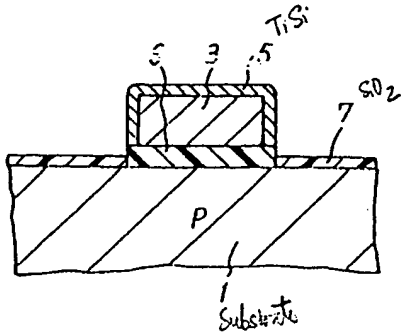


B

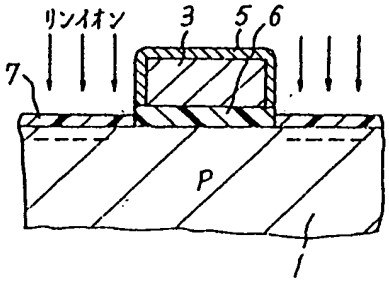


第 1 図

C

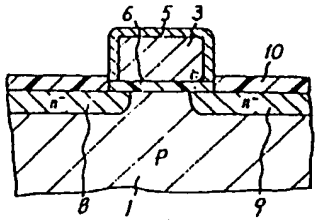


D

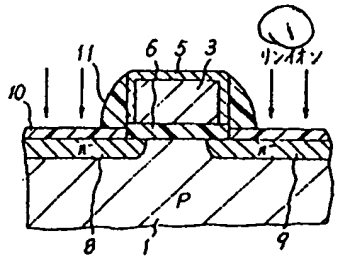


第 1 図

E



F



G